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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR		ATTORNEY DOCKET NO.
09/362,670	07/29/99	SANDER	B	032219-020

WM01/0425

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EXAMINER	
TSE, Y	
ART UNIT	**PAPER NUMBER**
2634	8

DATE MAILED: 04/25/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/362,670	Sander et al.
Examiner	**Art Unit**
Young Tse	2634

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *THREE* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jul 29, 1999*

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-8* is/are pending in the applica

4a) Of the above, claim(s) _____ is/are withdrawn from considera

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-8* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirem

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Claim 6 recites the limitation "the modulus" in line 8. There is insufficient antecedent basis for this limitation in the claim since it is unclear the first modulus or the second modulus.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Alberkrack et al..

Alberkrack et al. (U.S. Patent No. 4,121,162) discloses a phase locked loop (PLL) circuit in Figure 3. The PLL circuit includes a phase comparator (36), a tuning voltage generator (40), a tuner VCO (30), a programmable divider circuit (32), and a programmable divider controller (34). The programmable divider circuit (32) includes a prescaler (50), a variable modulus divider (52), a programmable counter (54), a data selector (56), a look ahead (58), and a divider (60) for determining the division operation and counting transitions of an applied frequency signal of the PLL circuit by the dividers or counters. The programmable divider controller (34) for controlling

or selecting the states of the counters, as recited in claims 1-8. Also see col. 3, line 53 to col. 4, line 35.

4. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Borras et al..

Borras et al. (U.S. Patent No. 4,484,153) discloses a phase locked loop (PLL) circuit in Figure 2. The PLL circuit includes a phase detector (34), a loop filter (40), a VCO (42), a programmable divider circuit which includes a prescaler (44), a binary up counter (46), and a pair of comparators or dividers (48 and 50), and a programmable divider controller includes a modulus controller (51), a divider range controller (64), and a pair of latches (56 and 58). The programmable divider circuit for determining the division operation, counting transitions of an applied frequency signal of the PLL circuit by the dividers or counters. The programmable divider controller for controlling or selecting the states of the counters, as recited in claims 1-8. Also see col. 4, lines 7-43.

5. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Bates et al..

Bates et al. (U.S. Patent No. 4,660,182) discloses a phase locked loop (PLL) circuit in Figure 1. The PLL circuit includes a phase detector (47), a loop filter (53), a low-pass active filter (55), a VCO (21), and a programmable divider circuit and a programmable divider controller (27). The programmable divider circuit may include a counter control logic circuit (31) and a plurality of counters (35, 37, and 39) and the programmable divider controller may include a dual modulus prescaler (29), a modulus control counter (33), and a plurality of switches (41, 43, and 45). The programmable divider circuit for determining the division operation and counting

transitions of an applied frequency signal of the PLL circuit by the counters. The programmable divider controller for controlling or selecting the states of the counters, as recited in claims 1-8. Also see col. 2, line 47 to col. 3, line 8.

6. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Fukuda.

Fukuda (U.S. Patent No. 5,424,687) discloses a phase locked loop (PLL) circuit in Figure 4. The PLL circuit includes a phase detector (5), a filter circuit (8), a VCO (1), and a fractional divider circuit (2). The fractional divider circuit includes counters (23-24 and 27-28) and a divider controller which may include a prescaler and a selector (25). The fractional divider circuit for determining the division operation, counting transitions of an applied frequency signal of the PLL circuit by the counters, and controlling or selecting the states of the counters, as recited in claims 1-8. Also see col. 7, line 67 to col. 8, line 38.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The prior art references Ooms (U.S. Patent No. 4,316,151), Cok et al. (U.S. Patent No. 4,573,023), Nakagawa et al. (U.S. Patent No. 4,864,634), Bradley (U.S. Patent No. 4,891,774), Kasturia (U.S. Patent No. 5,572,168), Nakagawa et al. (U.S. Patent No. 5,714,896), Sumi (U.S. Patent No. 5,729,179), and Wang (U.S. Patent No. 6,094,569) are made of record and related to a phase locked loop circuit including a phase detector, a filter circuit, a VCO, and a

programmable control circuit comprising dual modulus prescaler and counters for controlling or selecting a counter frequency to the phase detector.

Any response to this action should be mailed to:

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or faxed to:

(703) 308-9051 or (703) 308-9052, (for formal communications intended for entry)

Or:

(703) 308- 6743, (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Young Tse whose telephone number is (703) 305-4736. The examiner can normally be reached on Monday-Friday from 9:30 AM to 5:30 PM.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-4700.

Young T. Tse
Primary Examiner
April 20, 2001